

Materia

A pool of 8-bit bus modules with free routing.

Materia is a monolithic binary subsystem inspired by the Xaoc Leibniz: audio is quantized to bytes, pushed through counters, bit-flippers, logic gates, lookup tables and shift registers, and rebuilt by two DACs. It is inspired by, not faithful to, the hardware, and every extension is on by default.

Every module input, gate and clock picks its source from one shared bus list. A bus carries 8 data bits plus a clock level. Complete state (pipelines, counters, holds, oscillator phase, RNG) is saved with the Live set, presets and device duplicates.

DEFAULT PATCH

```
L -> ADC1 -> LP1 -> GER -> DAC A -> L
R -> ADC2 -> LP2 -----> DAC B -> R
```

Lipsk (LP) flips selected bits, Gera (GER) passes them (all on = identity), so the defaults are a plain 8-bit pass-through. Everything else is routing.

QUICK START

- 1 Load on an audio track with a source playing. The default patch is an 8-bit pass-through.
- 2 Open the **LP1** tab and toggle bits to flip them. Open **GER** and turn bits off to mask them.
- 3 Route an Erfurt counter into a Lipsk gate, or set **DAC A Source** to a module such as JEN or ROS1, and listen to the bus change.
- 4 Use **Berlin** as a byte oscillator, or set an ADC Clock to RATE for sample-rate reduction.
- 5 Use **TAP** tabs to map bus bits onto Live parameters for rhythm and slow control.

CONTROLS

MODULES

CONTROL	RANGE	WHAT IT DOES
ADC1, ADC2 (Drezno ADC)	L / R / Mid / Side in	Quantize audio to a byte. Gain +/-24 dB, Offset, Bipolar or Unipolar. Clock: CONT, RATE (1 Hz-96 kHz), BUS, ZERO-X (pitch-tracked). Silence quantizes to 128, so the DC block defaults on.
DAC A, DAC B (Drezno DAC)	sink	Rebuild audio from a bus. Weights: IDEAL, LADDER (seeded 0-25 % tolerance) or CUSTOM (per-bit weights). Gain -80 to +12 dB, Filter NONE / 1-pole / 4-pole, Cutoff, DC block, Destination L / R / Both.
BER (Berlin)	0.01 Hz-fs/2	Byte-phase oscillator at 110 Hz by default. Fine +/-100 ct, FM from DAC A, DAC B or track input, Clock STEP or CYCLE, sync source.

CONTROL	RANGE	WHAT IT DOES
ERF1, ERF2 (Erfurt)	registered	Accumulating counter. Step from CONST (1-255) or a bus, UP / DOWN, direction gate, reset source. Bit k with step 1 divides the clock by $2^{(k+1)}$. ERF1 defaults to an audio-rate divider off Berlin, ERF2 to a transport-synced rhythm counter.
LP1, LP2 (Lipsk)	combinational	Flips selected bits (Flip 0-7). A gate bus, with rotation and invert, forces or inverts flips by OR or XOR.
GER (Gera)	combinational	Masks bits with AND, OR, XOR or NAND. A lit toggle means pass. Same gate options as Lipsk.
JEN (Jena)	lookup	Generated tables, not a ROM clone. Families: Identity and bit ops, Folds, Walsh (sequency), Walsh (Hadamard), Shapes, Rhythm, User. Table index plus Morph; ASYNC or SYNC (latched on a clock edge).
ROS1, ROS2 (Rostock)	64-slot ring	Shift register. Length 1-64. Modes SHIFT, LOOP, SCRAMBLE, HOLD. Contents are saved with the set, so a LOOP pipeline is a stored pattern.
PZ (Poczdam)	switch	Selects A or B by hand, by a bus bit, or clocked. PZ.1 gets the selection, PZ.2 the other.
MTX (Bit Matrix)	combinational	8x8 bit routing with OR or XOR. Presets: Identity, Reverse, Gray, Rotate+1, Random perm, Custom.
TAP1-4	to Live params	Map a bus byte, a single bit, or a masked OR onto any Live parameter. With defaults they read ERF2 bits 0-3 at 1/16: square waves a 1/8 note, 1/4 note, 1/2 note and 1 bar long.

STATE AND CLOCKS

Transport clock (TCLK)	1/64 ... 8 bars	A transport-synced square on the bus list. Default 1/16. Stops with the transport.
Internal clock (ICLK)	0.01 Hz-96 kHz	Free-running square. Default 8 Hz.
Race handling	DELAY / LAST / NOISE	How combinational loops resolve. See below. Default DELAY.
Load state	RESUME / CLEAR PIPES / CLEAR ALL	What a Set load does with stored state.
Recall on play	OFF / S1 / S2	Restores a state slot on play for deterministic playback and export.
Constant	0-255	The CONST bus value.

NOTES

Bus list

ZERO, CONST, ADC1, ADC2, BER, ERF1, ERF2, LP1, LP2, GER, JEN, ROS1, ROS2, PZ.1, PZ.2, MTX, TCLK, ICLK, ERF1.OVF, ERF2.OVF, NOTE, VEL. NOTE and VEL read as zero in the audio effect. Routing parameters are automatable; mid-note switches are hard digital cuts.

Loops

Registered modules (ADC, ERF, ROS, clocked PZ and JEN) never race. A loop through only combinational modules (LP, GER, JEN async, PZ, MTX) has no stable state, so DELAY reads the previous sample on the back edge of the loop: stable, deterministic, audio-rate feedback. LAST takes the final of several settle passes. NOISE turns bits that still differ into seeded random bits.

Patches to try

- ERF1 step source = LP1 and LP1 source = ERF1: a pseudo-chaotic accumulator.

- ERF2 step source = ERF1: cascaded accumulators; ERF2 integrates ERF1's ramp.
- ROS2 source = ROS1, with ROS2 in LOOP at a different length: captured phrases recirculating against a live pipeline.
- Bit Matrix in XOR with a CUSTOM-weighted DAC is a Walsh synthesizer.

Notes

- Bus data is integers 0-255; ops wrap with `& 255`. No smoothing exists on the bus side; filtering lives after the DACs.
- Parameter modulation through TAPs is block-rate at best.
- At higher oversampling, Berlin STEP saturates higher and ADC CONT samples more often, which changes the sound.

STATUS

Spec v0.2. Offline scripts cover routing, defaults and ES5 compatibility, and there is a native QA patch. Confirm behaviour by loading in Live and listening.